AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently amended) A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising ~~the following method steps~~:

A) ~~provision of~~providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on ~~the~~ a surface of the semiconductor ~~surface~~;

B) ~~production of~~producing an insulator layer on the semiconductor surface;

C) ~~formation~~ forming ~~of~~ a sacrificial layer on the insulator layer, ~~the~~ where regions between the mutually adjacent gate electrode tracks are essentially ~~being~~ filled and the gate electrode tracks ~~being~~ are covered;

D) ~~formation of~~forming material plugs on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks;

E) ~~anisotropic~~ anistropically etching ~~of~~ the sacrificial layer, where the material plugs with the underlying sacrificial layer blocks ~~remaining~~;

F) ~~production of~~producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, where the regions between the mutually adjacent gate electrode tracks are essentially ~~being~~ filled and an essentially planar surface ~~being~~ is formed;

G) etching ~~of~~ sacrificial layer material from the vitreous layer for ~~the purpose of~~ removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) ~~removal of~~ removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling ~~of~~ the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer.

2. (Currently Amended) The method as claimed in claim 1, ~~method~~ step F) comprising the following ~~method~~ steps:

F1) ~~removal of~~removing the material plugs;

F2) ~~removal of~~removing the uncovered insulator layer on the semiconductor surface between the mutually adjacent gate electrode tracks;

F3) ~~production of~~producing dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for ~~the purpose of~~ forming the selection transistors;

F4) ~~production of~~producing a liner layer, which ~~preferably comprises~~includes silicon nitride;

F5) ~~formation of~~forming the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) ~~planarization~~ planarizing~~of~~ the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, thereby forming the essentially planar surface ~~being formed~~.

3. (Currently Amended) The method as claimed in claim 2, wherein the liner layer ~~being~~ is a ~~nitrogen-containing layer, preferably~~ silicon nitride layer or a silicon oxide-nitride layer.

4. (Currently Amended) The method as claimed in claim 2 ~~or 3~~, wherein the planarization in method step F6) ~~being~~ is effected by chemical mechanical polishing and the end point of the polishing operation being defined at the establishment of a material removal of the liner layer.

5. (Currently Amended) The method as claimed in ~~one of claims 1 to 4~~ claim 1, wherein the vitreous layer formed in method step F) ~~being~~ is a BPSG layer.

6. (Currently Amended) The method as claimed in ~~one of claims 1 to 5~~ claim 1, wherein method step C) ~~comprising~~ comprises~~the following method steps~~:

C1) ~~deposition of~~depositing a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

C2) ~~planarization of~~planarizing the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and

C3) ~~deposition of~~ depositing a second sacrificial layer.

7. (Currently Amended) The method as claimed in claim 6, wherein the second sacrificial layer ~~having~~ has a layer thickness of 200 nm to 1000 nm.

8. (Currently Amended) The method as claimed in ~~one of claims 1 to 5~~ claim 1, wherein ~~method~~ step C) ~~comprising~~ comprises~~the following method steps~~:

C1') ~~deposition of~~depositing the sacrificial layer on the insulator layer, where the regions between the mutually adjacent gate electrode tracks ~~being~~ are filled and the gate electrode tracks ~~being~~ are covered; and

C2') ~~planarization of~~planarizing the sacrificial layer, where the gate electrode tracks ~~remaining~~ remain covered and an essentially planar surface ~~being~~ is formed.

9. (Currently Amended) The method as claimed in claim 8, wherein the sacrificial layer ~~having~~ has a layer thickness of 200 nm to 1000 nm above the gate electrode tracks.

10. (Currently Amended) The method as claimed in ~~one of claims 1 to 9~~ claim 1, wherein the insulator layer ~~being~~ is a silicon dioxide layer.

11. (Currently Amended) The method as claimed in ~~one of claims 1 to 10~~ claim 1, wherein ~~method~~ step D) ~~comprising~~ comprises~~the following method steps~~:

D1) ~~deposition of~~depositing a resist layer;

D2) ~~exposure of~~exposing the resist layer by ~~means of~~ a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and

D3) ~~development of~~developing the resist layer ~~in order~~ to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks.

12. (Currently Amended) The method as claimed in claim 11, wherein an ARC layer ~~being~~ is applied on the sacrificial layer before the resist layer.

13. (Currently Amended) The method as claimed in ~~one of claims 1 to 10~~ claim 1, wherein ~~method~~ step D) ~~comprising the following method steps~~comprises:

D1') ~~deposition of~~depositing a hard mask layer on the sacrificial layer;

D2') ~~deposition of~~depositing a resist layer on the hard mask layer;

D3') ~~exposure of~~ exposing the resist layer by ~~means of~~ a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D4') ~~development of~~developing the resist layer ~~in order~~ to remove the exposed regions of the resist layer outside the contact openings between the mutually adjacent gate electrode tracks;

D5') ~~anisotropic~~ anistropically etching ~~of~~ the hard mask layer with the patterned resist layer as a mask; and

D8') ~~removal of~~removing the residual resist layer.

14. (Currently Amended) The method as claimed in ~~one of claims 1 to 10~~ claim 1, wherein ~~method~~ step D) ~~comprising the following method steps~~comprises:

D1'') ~~formation of~~forming a hard mask layer on the sacrificial layer;

D2'') ~~planarization of~~planarizing the hard mask layer;

D3'') ~~deposition of~~ depositing a resist layer on the hard mask layer;

D4'') ~~exposure of~~ exposing the resist layer by ~~means of~~ a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') ~~development of~~ developing the resist layer in order to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') ~~anisotropic~~ anistropically etching of the hard mask layer with the patterned resist layer as a mask;

D7'') ~~removal of~~removing the patterned resist layer;

D8'') ~~introduction of~~introducing a filling material into the etching openings in the hard mask layer; and

D9'') ~~removal of~~removing the hard mask layer ~~in order~~ to form the material plugs made from the filling material on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks.

15. (Currently Amended) The method as claimed in claim 14, wherein the hard mask layer ~~being~~ is a ~~vitreous layer, preferably a~~ BPSG layer, and the filling material ~~being~~ is an organic ARC material.

16. (Currently Amended) The method as claimed in ~~one of claims 1 to 15~~ claim 1, wherein the sacrificial layer ~~being~~ is a polysilicon layer.

17. (Currently Amended) The method as claimed in ~~one of claims 1 to 16~~ claim 1, wherein the sacrificial layer ~~being~~ is a carbon layer.

18. (Currently Amended) The method as claimed in claim 17, wherein a dielectric hard mask layer is additionally ~~being~~ provided on the carbon layer.

19. (Currently Amended) A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising ~~the following method steps~~:

A) ~~provision of~~providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on ~~the~~ a surface of the semiconductor ~~surface~~;

B) ~~production of~~producing an insulator layer on the semiconductor surface;

C) ~~formation of~~forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) ~~formation of~~ forming material plugs on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks;

E) ~~anisotropic~~ anistropically etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) ~~production of~~producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions

between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching ~~of~~ sacrificial layer material from the vitreous layer for ~~the purpose of~~ removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) ~~removal of~~ removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling ~~of~~ the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

~~method~~ step C) comprises ~~the following method steps~~:

C1') ~~deposition of~~ depositing a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

C2') ~~planarization of~~ planarizing the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and

C3') ~~deposition of~~ depositing a second sacrificial layer.

20. (Original) The method as claimed in claim 19, wherein the second sacrificial layer has a layer thickness of 200 nm to 1000 nm.

21. (Currently Amended) A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising ~~the following method steps~~:

A) ~~provision of~~ providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks ~~on~~ a surface of the semiconductor ~~surface~~;

B) ~~production~~ producing ~~of~~ an insulator layer on the semiconductor surface;

C) ~~formation of~~ forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) ~~formation of~~forming material plugs on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks;

E) ~~anisotropic~~ anistropically etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) ~~production of~~producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching ~~of~~ sacrificial layer material from the vitreous layer for ~~the purpose of~~ removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) ~~removal of~~removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) ~~filling of~~filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

~~method~~ step C) comprises ~~the following method steps~~:

C1'') ~~formation of~~forming a plane first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered; and

C3'') ~~deposition of~~ depositing a hard mask layer formed as a second sacrificial layer.

22. (Currently Amended) The method as claimed in claim 19, wherein ~~method~~ step D) comprises ~~the following method steps~~:

D1') ~~deposition of~~depositing a resist layer;

D2') ~~exposure of~~exposing the resist layer by ~~means of~~ a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and

D3) ~~development of~~developing the resist layer ~~in order~~ to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for

~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks.

23. (Original) The method as claimed in claim 22, wherein an ARC layer is applied on the sacrificial layer before the resist layer.

24. (Currently Amended) A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising ~~the following method steps~~:

A) ~~provision of~~providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on ~~the~~ a surface semiconductor ~~surface~~;

B) ~~production of~~ producing an insulator layer on the semiconductor surface;

C) ~~formation of~~forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) ~~formation of~~forming material plugs on the sacrificial layer for ~~the purpose of~~ defining contact openings between the mutually adjacent gate electrode tracks;

E) ~~anisotropic~~ anistropically etching ~~of~~ the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) ~~production of~~ producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) ~~etching of~~etching sacrificial layer material from the vitreous layer for ~~the purpose of~~ removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) ~~removal of~~removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling ~~of~~ the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

~~method~~ step D) comprises ~~the following method steps~~:

D1'') ~~formation of~~forming a hard mask layer on the sacrificial layer;

D2'') ~~planarization of~~ planarizing the hard mask layer;

D3'') ~~deposition of~~depositing a resist layer on the hard mask layer;

D4'') ~~exposure of~~exposing the resist layer by ~~means of~~ a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') ~~development of~~developing the resist layer ~~in order~~ to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') ~~anisotropic~~ anistropically etching of the hard mask layer with the patterned resist layer as a mask;

D7'') ~~removal of~~removing the patterned resist layer;

D8'') ~~introduction of~~introducing a filling material into the etching openings in the hard mask layer; and

D9'') ~~removal of~~removing the hard mask layer in order to form the material plugs made from the filling material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

25. (Currently Amended) The method as claimed in claim 24, wherein the hard mask layer is a ~~vitreous layer, preferably~~ a BPSG layer, and the filling material is an organic ARC material.

26. (previously presented)The method as claimed in claim 19, wherein the insulator layer is a silicon dioxide layer.

27. (Currently Amended) The method as claimed in claim 19, wherein ~~method~~ step F) comprises ~~the following steps~~:

F1) ~~removal of~~removing the material plugs;

F2) ~~removal of~~ removing the uncovered insulator layer on the semiconductor surface between the mutually adjacent gate electrode tracks;

F3) ~~production of~~producing dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for ~~the purpose of~~ forming the selection transistors;

F4) ~~production of~~producing a liner layer;

F5) ~~formation of~~forming the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) ~~planarization of~~planarizing the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the essentially planar surface being formed.

28. (Currently Amended) The method as claimed in claim 27, wherein the liner layer is a ~~nitrogen-containing layer, preferably~~ silicon nitride layer or a silicon oxide-nitride layer.

29. (Currently Amended) The method as claimed in claim 27, wherein the planarization in ~~method~~ step F6) is effected by chemical mechanical polishing and ~~the~~ an end point of the polishing operation is defined at the establishment of a material removal of the liner layer.

30. (Currently Amended) The method as claimed in claim 19, the vitreous layer formed in ~~method~~ step F) being a BPSG layer.